AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A semiconductor device, comprising:

a connection plug, defined by a via hole filled with a metal, comprising a nanomaterial surrounded by the metal, wherein,

the nanomaterial is substantially uniformly disposed in a section of the via hole, and

the metal both surrounds the nanomaterial and fills the via hole from a bottommost surface of the via hole to a topmost height of the via hole.

2. (currently amended) A semiconductor device comprising:

an insulating film (10);

an interlayer dielectric film (12) on the insulating film;

a trench within (11) the dielectric film; and

an interconnection comprising i) a metal layer (39) filling the trench from a bottommost surface of the trench to a

topmost height of the trench and ii) nanotubes (14) mixed in the metal layer,

wherein the nanotubes are of a nanomaterial substantially uniformly formed on a bottom surface of the interconnection.

3. (original) The semiconductor device according to claim 1, wherein the nanomaterial is a fibrous carbon nanomaterial, a particle-like carbon nanomaterial or a thin silicon wire.

4. (original) The semiconductor device according to claim 2, wherein the nanomaterial is a fibrous carbon nanomaterial, a granular particle-like carbon nanomaterial or a thin silicon wire.

5. (original) The semiconductor device according to claim 1, wherein the nanomaterial is oriented substantially perpendicularly to a substrate.

6. (original) The semiconductor device according to claim 2, wherein the nanomaterial is oriented substantially perpendicularly to a substrate.

7. (original) The semiconductor device according to claim 1, wherein the nanomaterial is provided in the whole connection plug.

8. (original) The semiconductor device according to claim 2, wherein the nanomaterial is provided up to the vicinity of a top surface of the interconnection.

9-19. (canceled)

20. (previously presented) The semiconductor device according to claim 1, wherein the metal layer is formed by a plating liquid comprising the nanomaterial.

21. (previously presented) The semiconductor device according to claim 2, wherein the metal layer is formed by a plating liquid comprising the nanomaterial.

22-26. (canceled)

27. (currently amended) A semiconductor device comprising:

an insulating film (10);

an interlayer dielectric film (12) on the insulating film;

a trench within (11) the dielectric film;

a first etching stopper layer (16) covering the dielectric film; and

an interconnection, comprising,

a metal layer (39) filling the trench[[;]],

a barrier metal layer (13) coating a bottom and sides of the trench, the barrier metal layer located intermediate the metal layer and the dielectric film with the barrier metal layer separating the metal layer from the dielectric film[[;]],

particles of metal (15) on a lower horizontal surface of the barrier metal layer[[;]], and

carbon nanotubes (14) formed on the metal particles and mixed in the metal layer,

wherein, each of i) the trench (11), ii) the interconnection, iii) the metal layer (39), iv) the barrier metal layer (13), and the carbon nanotubes (14) extend through the first etching stopper layer.

28. (cancelled)

29. (currently amended) The semiconductor device according to claim [[28]] 27, further comprising:

a second etching stopper layer (27) formed on the etching stopper layer (16), on the barrier metal layer (13), and on part of the metal layer (39);

another interlayer dielectric film (29) formed on the second etching stopper layer;

a third etching stopper layer (30) formed on the another dielectric film;

a via hole formed in the second etching stopper layer, the another dielectric film, and the third etching stopper layer;

metal (26) filling the via hole;

another barrier metal layer (28) covering a bottom and sides of the via hole and extending up to a top of the another dielectric film, the another barrier metal layer separating the metal filling the via hole from the bottom and sides of the via hole;

further metal particles on the another barrier metal layer covering the bottom of the via hole;

further carbon nanotubes (24) formed on further the metal particles and mixed in the metal filling the via hole,

wherein, said metal filling the via hole, said further carbon nanotubes, and said another barrier metal layer define a connection plug contacting said interconnection.